Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

BEC001 – Advanced Computer Architecture
Fifth Semester, 2016-17 (odd Semester)

Course (catalog) description

To make students know about the Parallelism concepts in Programming. To give the students an elaborate idea about the different memory systems and buses. To introduce the advanced processor architectures to the students. To make the students know about the importance of multiprocessor and multi-computers. To study about data flow computer architectures

Compulsory/Elective course: Elective for ECE Students

Credit hours **: 3** credits

Course Coordinator **:** G.Kanagavalli, Asst. Professor, Department of ECE

Instructors **:**

Name of the instructor	Class handling	Office location	Office phone	Email (domain:@ bharathuniv.ac.in	Consultation
Ms. G.Kanagavalli	III year ECE	SA020		Kanagavalli.ece@ bharathuniv.ac.in	12.30-1.30 pm

Relationship to other courses:

Pre –requisites **:** BCS101- Fundamentals of computing and programming

Assumed knowledge : The students will have a basic knowledge in operation of digital computer, concept of pipelining and memory system including cache memories and virtual memory

Following courses : BET008 - Wireless Networks

Syllabus Contents

UNIT- I **9**

PARALLEL COMPUTER MODELS

Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl‘s law, Gustafson‘s law-Memory bounded speedup Model.

UNIT- II **9**

MEMORY SYSTEMS AND BUSES

Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization -Interleaved memory organization, Lower order interleaving, Higher order interleaving. Back plane bus systems-Bus addressing, arbitration and transaction.

UNIT -III **9**

ADVANCED PROCESSORS

Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture- Multivector and SIMD computers-Vector processing principles-Cray Y-MP 816 system -Inter processor communication

UNIT- IV **9**

MULTI PROCESSOR AND MULTI COMPUTERS

Multiprocessor system interconnects- Cross bar switch, Multiport memory-Hot spot problem, Message passing mechanisms-Pipelined processors-Linear pipeline, on linear pipeline-Instruction pipeline design -Arithmetic pipeline design.

UNIT- V **9**

DATA FLOW COMPUTERS AND VLSI COMPUTATIONS

Data flow computer architectures-Static, Dynamic-VLSI Computing Structures-Systolic array architecture, mapping algorithms into systolic arrays, Reconfigurable processor array-VLSI matrix arithmetic processors -VLSI arithmetic models, partitioned matrix algorithms, matrix arithmetic pipelines.

TOTAL NO OF PERIODS: 45

TEXT BOOKS:

1. Kai Hwang, Advanced Computer architecture Parallelism ,scalablity ,Programmablity ,Mc Graw Hill,N.Y, 2003
2. Kai Hwang and F.A.Briggs, Computer architecture and parallel processor ' Mc Graw Hill, N.Y, 1999

REFERENCES:

1. David A. Patterson and John L. Hennessey, —Computer organization and design Elsevier,
2. Fifth edition, 2014.
3. **www.sci.tamucc.edu/~sking/Courses/COSC5351/syllabus.php**

Computer usage: Nil

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area : Communication | Signal Processing | Electronics | VLSI | Embedded | **Computer**

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	August 1st week	Session 1 to 14	2 Periods
2	Cycle Test-2	September 2nd week	Session 15 to 28	2 Periods
3	Model Test	October 2nd week	Session 1 to 45	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

To make students know about the Parallelism concepts in Programming .To give the students an elaborate idea about the different memory systems and buses. To introduce the advanced processor architectures to the students. To make the students know about the importance of multiprocessor and multi-computers. To study about data flow computer architectures .	Correlates to program outcome		
	H	M	L
Demonstrate concepts of parallelism in hardware/software.	b	d, e	a
Discuss memory organization and mapping techniques.	d	e	c
Describe architectural features of advanced processors.	b	c	a
Interpret performance of different pipelined processors.	e	c	a
Explain data flow in arithmetic algorithms	e	c	a
Development of software to solve computationally intensive problems.	d	b	a

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture Schedule

Session	Topics	Problem solving (Yes/No)	Text / Chapter
UNIT I PARALLEL COMPUTER MODELS			
1.	Evolution of Computer architecture	No	[T1] Chapter -1
2.	system attributes to performance		
3.	Multi processors and multi computers		
4.	Multi-vector and SIMD computers	No	
5.	PRAM and VLSI models-Parallelism in Programming	No	
6.	conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms	No	
7.	Speed up performance laws-Amdahl‘s law	No	
8.	Gustafson‘s law	No	
9.	Memory bounded speedup Model	No	
UNIT II MEMORY SYSTEMS AND BUSES			
10.	Memory hierarchy	No	[T1] Chapter -2
11.	Cache and shared memory concepts	No	
12.	Cache memory organization	No	
13.	Cache addressing models	No	
14.	Aliasing problem in cache	No	
15.	Cache memory mapping techniques .	No	
16.	Shared memory organization-Interleaved memory organization .	No	
17.	Lower order interleaving, Higher order interleaving	No	
18.	Back plane bus systems	No	
19.	Bus addressing, arbitration and transaction	No	
UNIT III ADVANCED PROCESSORS			
20.	Instruction set architectures	No	[T1] Chapter -3
21.	CISC and RISC scalar processors	No	
22.	Super scalar processors	No	
23.	VLIW architecture	No	
24.	Multivector and SIMD computers	No	
25.	Vector processing principles	No	
26.	Cray Y	No	

27.	MP 816 system	No	
28.	Inter processor communication	No	
UNIT IV MULTI PROCESSOR AND MULTI COMPUTERS			
29.	Multiprocessor system interconnects	No	[T1] Chapter -4
30.	Cross bar switch	No	
31.	Multiport memory	No	
32.	Hot spot problem	No	
33.	Message passing mechanisms	No	
34.	Pipelined processors-Linear pipeline	No	
35.	on linear pipeline	No	
36.	Instruction pipeline design	No	
37.	Arithmetic pipeline design	No	
UNIT V **DATA FLOW COMPUTERS AND VLSI COMPUTATIONS**			
38.	Data flow computer architectures	No	[T1] Chapter -5
39.	Static, Dynamic	No	
40.	VLSI Computing Structures	No	
41.	Systolic array architecture	No	
42.	mapping algorithms into systolic arrays	No	
43.	Reconfigurable processor array	No	
43.	VLSI matrix arithmetic processors	No	
44.	VLSI arithmetic models	No	
45.	partitioned matrix algorithms, matrix arithmetic pipelines	No	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures

- Laboratory sessions, which support the formal lecture material and also provide the student with practical construction, measurement and debugging skills.

- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	10%
Cycle Test – II	-	10%
Model Test	-	25%
Attendance	-	5%
Final exam	-	50%

Prepared by: G.Kanagavalli, Assistant Professor, Department of ECE Dated: 10/7/2017

Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate:

Engineering Graduate will have

a)an ability to apply knowledge of mathematics, science, and engineering fundamentals.

b)an ability to identify, formulate, and solve engineering problems

c)an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

d)an ability to design and conduct experiments, as well as to analyze and interpret data

e)an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

f)an ability to apply reasoning informed by a knowledge of contemporary issues

g)an ability to broaden the education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context

h) an ability in understanding of professional and ethical responsibility and apply them in engineering practices

i) an ability to function on multidisciplinary teams

j) an ability to communicate effectively with the engineering community and with society at large

k) an ability in understanding of the engineering and management principles and apply them in Project and finance management as a leader and a member in a team.

Program Educational Objectives

PEO1: PREPARATION:

To provide strong foundation in mathematical, scientific and engineering fundamentals necessary to analyze, formulate and solve engineering problems in the field of Electronics And Communication Engineering.

PEO2: CORE COMPETENCE:

To enhance the skills and experience in defining problems in Electronics And Communication Engineering design and implement, analyzing the experimental evaluations, and finally making appropriate decisions.

PEO3: PROFESSIONALISM:

To enhance their skills and embrace new Electronics And Communication Engineering Technologies through self-directed professional development and post-graduate training or education

PEO4: SKILL:

To provide training for developing soft skills such as proficiency in many languages, technical communication, verbal, logical, analytical, comprehension, team building, inter personal relationship, group discussion and leadership skill to become a better professional.

PEO5: ETHICS:

Apply the ethical and social aspects of modern communication technologies to the design, development, and usage of electronics engineering.

Course Teacher	Signature
Ms. G.KANAGAVALLI	

Course Coordinator	Academic Coordinator	Professor In-Charge	HOD/ECE
(Ms.G.Kanagavalli)	( )	(Dr.)	( )